DUAL 100 BIT DYNAMIC SHIFT REGISTER

- **Low Power Dissipation--.4 mW/bit at 1 MHz**
- **High Frequency Operation -- 2 MHz Guaranteed over Temperature Range**
- **DTL, TTL Compatible**
- **Low Clock Capacitance -- 40 pF**
- **Low Clock Leakage -- ≤.5 μA at —18 V**
- **Inputs Protected Against Static Charge**
- **Standard Packaging -- Low Profile TO-5**
- **Military and Commercial Temperature Ranges**
- **Low Output Impedance -- 300Ω Typical**

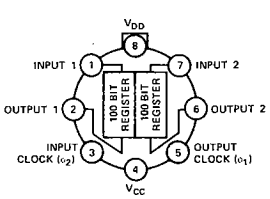
The Intel dual 100 bit dynamic shift register element consists of normally off P-channel MOS devices integrated on a monolithic array. It uses low voltage circuitry to minimize power dissipation and to facilitate interfacing with bipolar integrated circuits. It uses two clock phases only.

The dual 100 bit device can be driven directly by standard bipolar integrated circuits (TTL, DTL, etc.) or by MOS circuits. The design of the output stage provides driving capability for MOS or bipolar IC's.

Use of the low threshold **silicon gate technology** allows high speed (2 MHz guaranteed), while reducing power dissipation by a factor of 2 and reducing clock input capacitance by a factor of 3 compared to equivalent products manufactured by conventional MOS technologies.

This family is designed for low cost buffer applications. It is available in both military (—55°C to +125°C) and industrial (0°C to +70°C) grade. It is also available with or without an internal 20K pull-up resistor which may provide easier interfacing to other circuitry.

PIN CONFIGURATION



Configuration	Open Drain Output		20kΩ Output	
	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Dual 100 Bit	1406	1506	1407	1507

Absolute Maximum Ratings*

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +160°C
Power Dissipation (1)	500 mW
Data and Clock Input Voltages with Respect to Most Positive Supply Voltage, V_{CC}	+.5 V to −25 V
Power Supply Voltage, V_{DD} with Respect to V_{CC}	+.5 V to −25 V

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics

$\left[\begin{array}{l} T_A = -55°C \text{ to } +125°C \text{ (1406 and 1407)} \\ T_A = 0°C \text{ to } 70°C \text{ (1506 and 1507);} \end{array}\right]$ $V_{CC} = +5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$ unless otherwise noted.

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (5)	MAX.	UNIT	CONDITION
I_{LI}	INPUT LOAD CURRENT (PIN 1)			500	nA	GND ON PINS 2, 3, 4, 5, 6, 7 PIN 1 = −18V, PIN 8 = −8V $T_A = 25°C$
I_{LI}	INPUT LOAD CURRENT (PIN 7)			500	nA	GND ON PINS 1, 2, 3, 4, 5, 6 PIN 7 = −18V, PIN 8 = −8V $T_A = 25°C$
I_{LO} (2, 3)	OUTPUT LEAKAGE CURRENT (PIN 2)			500	nA	GND ON PINS 1, 4, 6, 7, 8 PIN 2 = −18V, PINS 3, 5 = −8V $T_A = 25°C$
I_{LO} (2, 3)	OUTPUT LEAKAGE CURRENT (PIN 6)			500	nA	GND ON PINS 1, 2, 4, 7, 8 PIN 6 = −18V, PINS 3, 5 = −8V $T_A = 25°C$
I_{LC}	CLOCK LEAKAGE CURRENT (PIN 3 OR PIN 5)			500	nA	PIN 3, PIN 5 = −18V; PIN 8 = −10V ALL OTHERS AT GND $T_A = 25°C$
I_{DD1}	POWER SUPPLY CURRENT, V_{DD}		10	17	mA	$T_A = -55°C$ } FREQ. = 1 MHz, 30% CLOCK DUTY CYCLE (SEE NOTE 4)
I_{DD2}	POWER SUPPLY CURRENT, V_{DD}		6.0	13	mA	$T_A = 0°C$ }
I_{DD3}	POWER SUPPLY CURRENT, V_{DD}		5.0	11	mA	$T_A = 25°C$ }
V_{IL}	INPUT "LOW" VOLTAGE	−10	+0.2	+0.8	V	$V_{DD} = -5V$, $V_{CC} = +5V$
V_{IH}	INPUT "HIGH" VOLTAGE	+2.5		+5.3	V	$V_{DD} = -5V$, $V_{CC} = +5V$
V_{IHC}	CLOCK INPUT "HIGH" LEVEL	+3.5		+5.3	V	$V_{DD} = -5V$, $V_{CC} = +5V$
V_{ILC}	CLOCK INPUT "LOW" LEVEL	−13		−9.5	V	$V_{DD} = -5V$, $V_{CC} = +5V$
Z_{OUT}	OUTPUT IMPEDANCE		300	750	Ω	$V_{DD} = -5V$, $V_{CC} = +5V$ $I_{SOURCE} = 2.5mA$
V_{OL}	OUTPUT "LOW" VOLTAGE		−1.8	0.4	V	$I_{OL} = 1.6$ mA SEE PAGE 7 FOR R_L
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.5	4		V	$I_{OH} = -100\ \mu A$ SEE PAGE 7 FOR R_L

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150° C/W junction to ambient. The full rating applies for ambient temperatures to +125°C for 1406, 1407 and +70°C for 1506, 1507.

Note 2: For 1407 and 1507 the output on pins 2 and 6 will exhibit a resistance when measured with the following bias conditions: pins 3, 4, and 8 at GND; pin 5 at −15V; pins 1, 7 open; measure pins 2 and 6. $25k\Omega \geq R_{OUT} \geq 15k\Omega$.

Note 3: Not for devices having internal resistors (1407 and 1507).

Note 4: In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle $= [t_{\phi PW} + \frac{1}{2}(t_R + t_F)] \times$ clock rate.

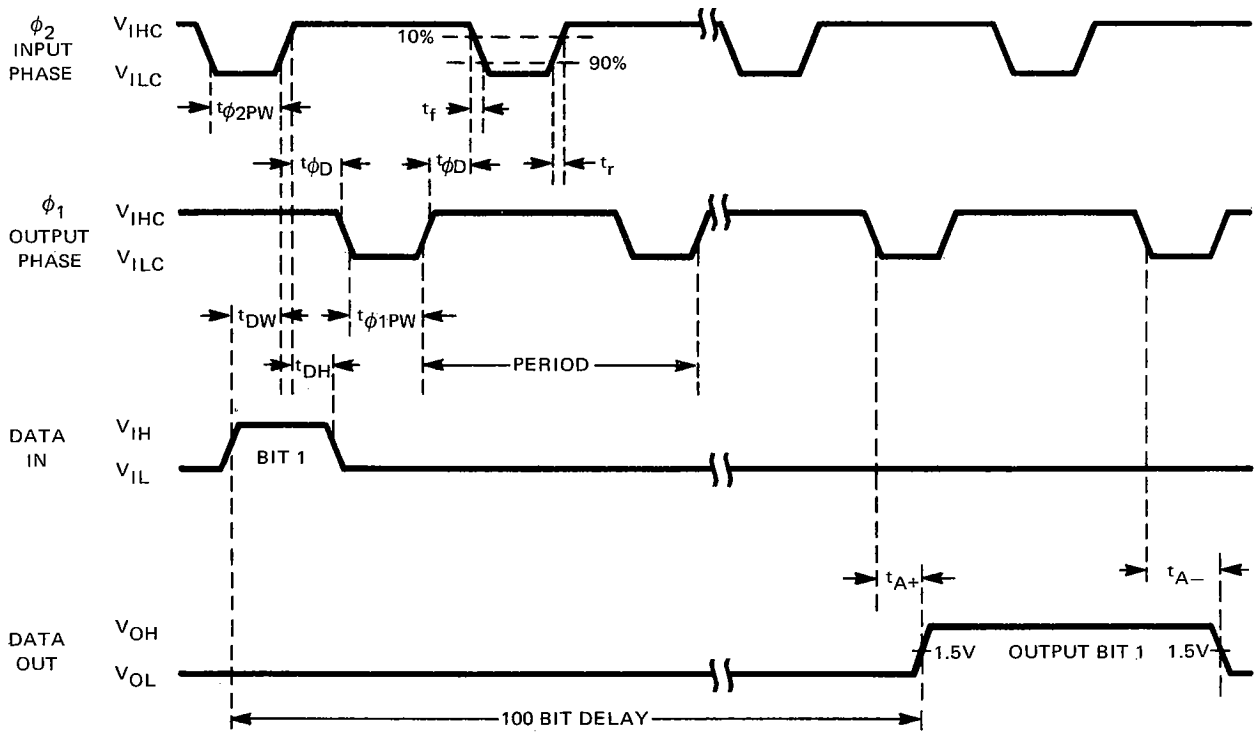
Note 5: Typical values are at 25°C and at nominal voltage.

Switching Characteristics

Conditions of Test

Data amplitude +.8 to +2.5V
Input rise and fall times: 10 nsec
Output load is 1 TTL gate

Timing Diagram



A.C. Characteristics $V_{DD} = -5V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, 1 TTL Load, $C_{TOTAL} = 20$ pF.

	1406	1506	1407	1507
T_A	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
R_L	3K	3K	3.6K	3.6K

SYMBOL	PARAMETER	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	(NOTE 1)	2	MHz	
$t_{\phi 1PW}$	ϕ_1 CLOCK PULSE WIDTH	130		ns	
$t_{\phi 2PW}$	ϕ_2 CLOCK PULSE WIDTH	130		ns	
$t_{\phi D}$	CLOCK PULSE DELAY	100		ns	
t_r, t_f	CLOCK PULSE TRANSITION		50	ns	@ 1 MHz
t_{DW}	DATA WRITE TIME (SET UP)	100		ns	
t_{DH}	DATA TO CLOCK HOLD TIME	100		ns	
t_{A+}, t_{A-}	CLOCK TO DATA OUTPUT DELAY		100	ns	$V_{ILC} - V_{CC} = -16V$

Capacitance[2], $T_A = 25°C$

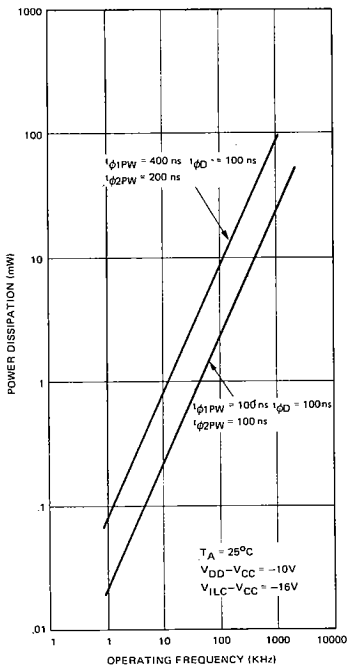
SYMBOL	PARAMETER	LIMIT TYP.	LIMIT MAX.	UNIT	CONDITION
C_{IN}	INPUT CAPACITANCE (PINS 1, 7)		4	pF	$V_{IN} = V_{CC}$
C_ϕ	CLOCK INPUT CAPACITANCE (PINS 3, 5)		40	pF	$V_\phi = V_{CC}$
C_ϕ	CLOCK INPUT CAPACITANCE (PINS 3, 5)		35	pF	$V_\phi = -20$ VOLT BIAS
$C_{\phi 1 \phi 2}$	CLOCK TO CLOCK CAPACITANCE	2	4	pF	$V_\phi = V_{CC}$
C_{OUT}	OUTPUT CAPACITANCE		5	pF	$V_{OUT} = V_{CC}$

Note 1: See page 6 for guaranteed curve

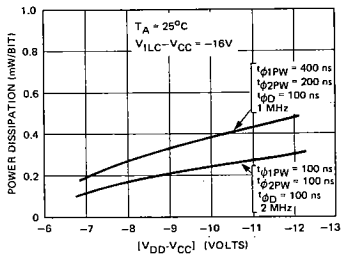
Note 2: This parameter is periodically sampled and is not 100% tested.

Typical Characteristics

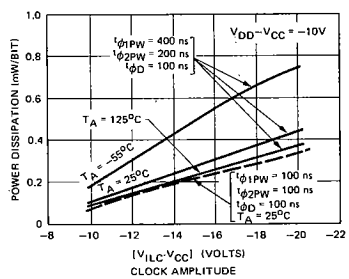
Power Dissipation vs Frequency



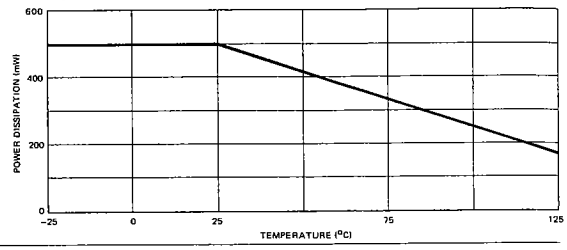
Power Dissipation/Bit vs Supply Voltage



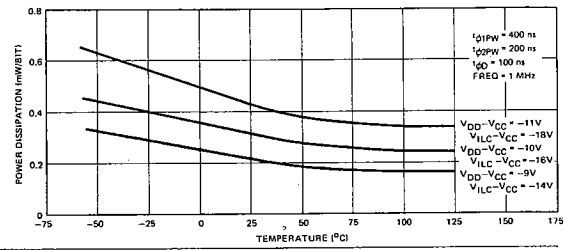
Power Dissipation/Bit vs Clock Amplitude



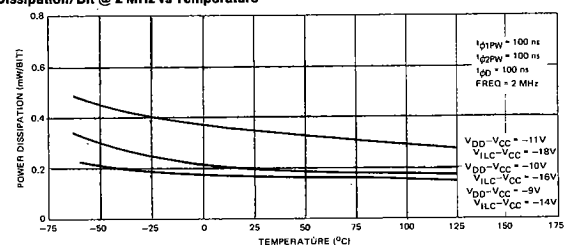
Maximum Package Power Dissipation



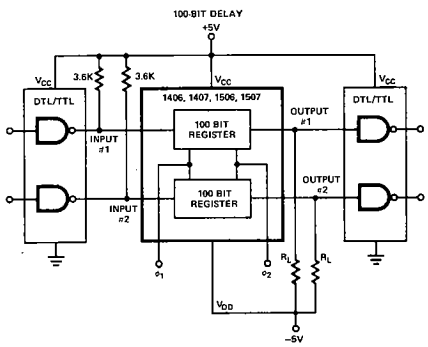
Power Dissipation/Bit @ 1 MHz vs Temperature

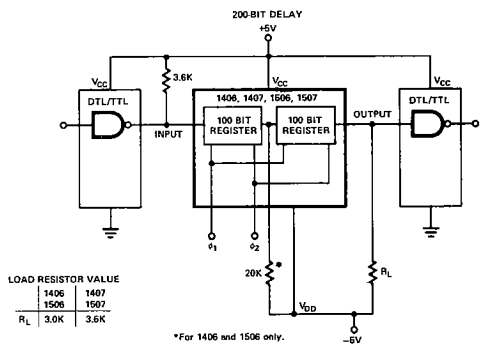


Power Dissipation/Bit @ 2 MHz vs Temperature



DTL/TTL MOS Interfaces

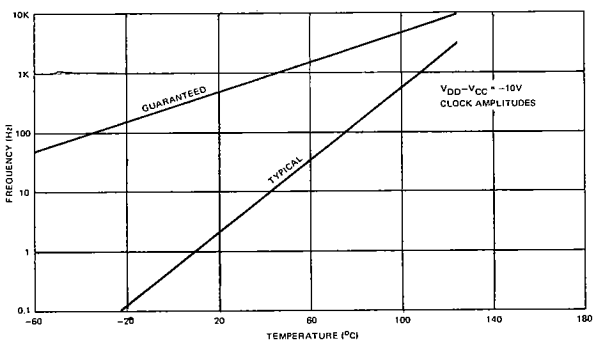




LOAD RESISTOR VALUE

	1406	1407
	1506	1507
R_L	3.0K	3.6K

Minimum Operating Frequency



Clock Amplitude vs Maximum Frequency